**CS 5122-00** Spring 2025

**VLSI Design for Manufacturability**

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**Course Content**

We have seen an incredible increase in the achievable density, performance, and complexity of integrated circuits. It is the result of the IC industry's continuous scaling of the minimum feature size. However, there are many challenges in maintaining the aggressive pace of technology scaling. Chip fabrication has become increasingly difficult with various kinds of manufacturing effects surfacing. As a result, many more manufacturing design rules are added and more sophisticated design methodologies are introduced. Manufacturing-aware physical design is necessary to ensure chip manufacturability and guarantee the yield.

Besides, the conventional 193nm immersion (193i) lithography with single exposure has already reached its printability limit at the 28nm technology node. To extend Moore’s Law, different solutions like extensions of 193 immersion with multiple patterning, extreme ultraviolet (EUV) lithography, directed self-assembly (DSA), nanoimprint, and electron beam (e-beam) lithography have been and are still being actively explored by the semiconductor industry.

In this course, we will introduce manufacturing-aware physical design. We will examine some representative research works in this area and learn a variety of algorithmic techniques for solving these challenging problems efficiently.

This course will be of interest to three types of students:

1. Students interested in integrated circuit design and manufacturing.

2. Students interested in software design. Many of the optimization algorithms we will talk about (A\*-search, linear programming, integer linear programming, dynamic programming, different graph algorithms, Monte Carlo algorithm, satisfiability, etc.) have many applications outside of CAD tool design. Understanding these algorithms is an essential component of any software designer's arsenal.

3. Students interested in pursuing research in CAD tool design. This is an exciting, fast moving area with many research opportunities.

**Class webpage** NTHU e-learning system <http://eeclass.nthu.edu.tw/>

**Textbook** No required textbook.

Lecture notes prepared by the instructor will be provided.

Supplemented with selected research papers.

**Schedule**

1. Maze Routing under Nanometer Design Rules

2. Redundant Via Insertion

3. Dummy Fill Insertion

4. Detailed Placement Refinement for Complex Manufacturing Constraints

5. Lithography Hotspot Detection

6. Double/Triple Patterning-Aware Physical Design (layout decomposition, routing, detailed placement)

7. Self-Aligned Double Patterning (SADP)-Aware Physical Design (layout decomposition, routing)

8. Layout Decomposition and Mask Optimization

9. E-Beam Direct Write/Mask Writing

10. Optimization with Hybrid Lithography (Multiple Patterning/Directed Self-Assembly/e-beam)

11. Extreme Ultraviolet (EUV) Lithography Optimization

**Grading** Assignments: 40%

Project: 30%

Exam: 30%

**General Policies**

1. Discussions of homework problems with other students are encouraged. However, every student MUST do his/her own work and write up the solutions independently.

2. A 10% late penalty per day will be applied to all late assignments. Assignments should be turned in at the beginning of class on the due date.

3. Students who violate University rules on scholastic dishonesty are subject to disciplinary penalties, including the possibility of failure in the course and/or dismissal from the University. Since such dishonesty harms the individual, all students, and the integrity of The University, policies on scholastic dishonesty will be strictly enforced.